

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
9 June 2005 (09.06.2005)

PCT

(10) International Publication Number
WO 2005/053026 A1

(51) International Patent Classification⁷: H01L 27/00, 21/77, H01G 4/33

(21) International Application Number: PCT/CA2004/002053

(22) International Filing Date: 29 November 2004 (29.11.2004)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data: 60/525,897 28 November 2003 (28.11.2003) US

(71) Applicant (for all designated States except US): GENNUM CORPORATION [CA/CA]; 970 Fraser Drive, Burlington, Ontario L7L 5P5 (CA).

(72) Inventors; and

(75) Inventors/Applicants (for US only): KOUTSAROFF, Ivoyl, P. [CA/CA]; 409-325 A James Street South, Hamilton, Ontario L8P 3B6 (CA). VANDERMEULEN, Mark [CA/CA]; #321-2030 Cleaver Avenue, Burlington, Ontario

L7M 4C3 (CA). CERVIN-LAWRY, Andrew [CA/CA]; 1101 Springbrook Crescent, Oakville, Ontario L6M 2C6 (CA). PATEL, Atin, J. [CA/CA]; 1520 Stillriver Crescent, Mississauga, Ontario L5M 3V4 (CA).

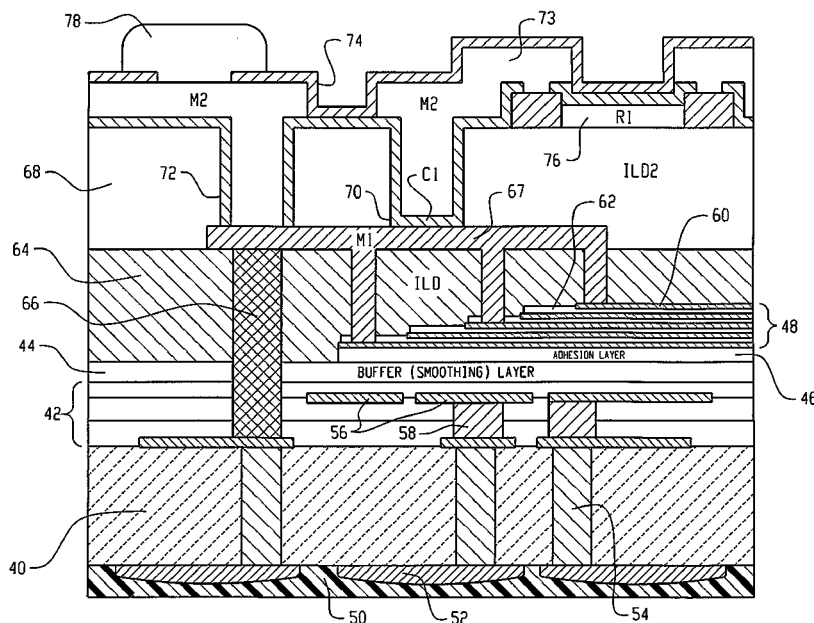
(74) Agents: PERRY, Stephen, J. et al.; SIM & McBURNEY, 330 University Avenue, 6th Floor, Toronto, Ontario M5G 1R7 (CA).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI,

[Continued on next page]

(54) Title: MULTI-LEVEL THIN FILM CAPACITOR ON A CERAMIC SUBSTRATE AND METHOD OF MANUFACTURING THE SAME



(57) Abstract: In accordance with the teachings described herein, a multi-level thin film capacitor on a ceramic substrate and method of manufacturing the same are provided. The multi-level thin film capacitor (MLC) may include at least one high permittivity dielectric layer between at least two electrode layers, the electrode layers being formed from a conductive thin film material. A buffer layer may be included between the ceramic substrate and the thin film MLC. The buffer layer may have a smooth surface with a surface roughness (Ra) less than or equal to 0.08 micrometers (um).

WO 2005/053026 A1



FR, GB, GR, HU, IE, IS, IT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

Published:

— *with international search report*

**Multi-Level Thin Film Capacitor On A Ceramic Substrate
And Method Of Manufacturing The Same**

FIELD

The technology described in this patent document relates generally to the field of thin film devices and fabrication. More particularly, the patent document describes a multi-level thin-film capacitor fabricated on a ceramic substrate and a method of manufacturing the same.

BACKGROUND AND SUMMARY

Thin film circuit packages are commonly used in space-constrained applications, such as hearing instrument products. In accordance with the teachings described herein, a multi-level thin film capacitor on a ceramic substrate and method of manufacturing the same are provided. The multi-level thin film capacitor (MLC) may include at least one high permittivity dielectric layer between at least two electrode layers, the electrode layers being formed from a conductive thin film material. A buffer layer may be included between the ceramic substrate and the thin film MLC. The buffer layer may have a smooth surface with a surface roughness (Ra) less than or equal to 0.08 micrometers (μm).

In another embodiment, a thin film integrated circuit may include a ceramic substrate and a plurality of passive thin film devices fabricated on the ceramic substrate. The plurality of passive thin film devices may include a tunable thin film multi-level capacitor (MLC) that includes at least one dielectric layer between at least two electrode layers. The dielectric layer(s) may include low, intermediate and/or high permittivity dielectric layers.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a diagram of an example multi-level thin film capacitor fabricated on a ceramic substrate.

Figure 2 is a diagram of an example multi-level thin film capacitor fabricated on a ceramic substrate including a high density interconnect (HDI) layer.

Figure 3 is a diagram of an example multi-level thin film capacitor fabricated on a ceramic substrate and integrated with a thin film circuit.

Figure 4 is a diagram of an example capacitor network integrating a thin film circuit including a high density multi-level thin film capacitor and a low density capacitor on a ceramic substrate with a high density thick film interconnect.

Figures 5-9 illustrate example processes for fabricating the circuit structure of Figure 4.

DETAILED DESCRIPTION

Figure 1 is a diagram of an example multi-level thin film capacitor 14 fabricated on a ceramic substrate 10. Also illustrated in Figure 1 is a buffer (smoothing) layer 12 fabricated between the ceramic substrate 10 and the multi-level capacitor (MLC) 14. A thin film MLC includes one or more layers of high permittivity dielectric material (e.g., compounds containing Barium Strontium Titanium Oxide (Ba, Sr)TiO₃, (BST)) deposited between electrode layers formed from a conductive thin film material (e.g., Pt, conductive oxides like, SrRuO₃, LaNiO₃, LaMn_{1-x}Co_xO₃, etc., other metals, like Au, Cu, W, etc.). The MLC 14 can be fabricated with a variety of capacitance-voltage characteristics depending on the material properties and processing conditions of the whole stack. The MLC 14 may include a voltage variable (tunable) capacitor(s) and/or a fixed value capacitor(s), depending on the type of dielectric material used for the dielectric layer(s). The MLC 14 may be a mesa-structure formed using photolithography patterning techniques (see, e.g., Figure 4). The fabrication of

a high value thin film capacitor (e.g., with an overall capacitance density from 10 to 390 fF/ μm^2) requires a high degree of precision, which typically cannot be achieved on a rough substrate material such as ceramic. A smooth surface sufficient for fabricating the MLC 14 is provided by the buffer layer 12.

The buffer layer 12 is a dielectric material that electrically isolates the thin film capacitor 14 and provides a smooth surface which is suitable for fabricating a thin film MLC 14. For example, the buffer layer 12 may be a thick film dielectric material that is polished to provide a smooth upper surface (see, e.g., Figure 7). In another example, the buffer layer 12 may be a smooth (fire polished) glass dielectric material (see, e.g., Figure 8). In the case of a polished thick film buffer layer (e.g., Figure 7), the surface roughness (R_a) of the smooth upper surface may be less than or equal to 0.08 micrometers (μm), but is preferably less than or equal to 0.06 μm . In the case of a glass dielectric buffer layer (e.g., Figure 8), the surface roughness (R_a) of the smooth upper surface may be less than or equal to 0.08 μm , but is preferably less than or equal to 0.03 μm . In addition to providing a low surface roughness (e.g., $R_a \leq 0.08\mu\text{m}$), the buffer layer 12 is substantially free of micropores and is thus stable at high temperatures. For example, the buffer layer 12 may be able to withstand multiple anneals at high temperatures (e.g., 600-800° C) in an oxidizing atmosphere without substantially affecting its surface quality or the resistivity of any metal filled vias. As a result, the high-k ferroelectric layer(s) of the MLC 14 may be deposited using a simple spin-coat technology, as well as methods such as Physical Vapor Deposition (PVD) or Chemical Vapor Deposition (CVD).

The ceramic substrate 10 may, for example, be Al_2O_3 , AlN , MgTiO_3 , Mg_2SiO_4 or some other ceramic substrate material. Ceramic substrate materials are typically inexpensive and are highly machinable. The ceramic substrate 10 may therefore include fine-pitched metal filled through holes that provide low and controlled parasitics (see, e.g., Figure 4). In

addition, a ceramic substrate material provides substantially better Q-factors for other passive components (e.g. thin film inductors) than conventional silicon-based substrates.

Figure 2 is a diagram of an example multi-level thin film capacitor 26 fabricated on a ceramic substrate 20 including a HDI layer 22. The HDI layer 22 is fabricated on the ceramic substrate using thick film materials and photolithography patterning techniques to create one or more layers of high density routing (i.e., metallic traces) and filled through holes (vias). In addition, the HDI layer 22 may include buried resistors and/or capacitors. The HDI layer 24 may, for example, be used to provide substrate level interconnect and electrical connections from the top to the bottom side of the substrate. The use of a low cost and high density thick film based interconnect layer is enabled by the use of a ceramic substrate material.

Figure 3 is a diagram of an example multi-level thin film capacitor 36 fabricated on a ceramic substrate 30 and integrated with a thin film circuit 38. The MLC 36 may be interconnected in a thin film circuit 38 with other passive thin film circuit elements, such as decoupling capacitors, inductors, resistors, etc. Also illustrated in Figure 3 is an adhesion layer 34 between the buffer layer 32 and the MLC 36. The adhesion layer 34 may be included to adhere the bottom electrode layer of the MLC 36 to the smooth surface of the buffer layer 34. The adhesion layer 34 may, for example, include one or more layers of thin film TiOx and/or Al₂O₃.

Figure 4 is a diagram of an example capacitor network integrating a thin film circuit including a high density thin film MLC 48 and a low density capacitor (C1) on a ceramic substrate 40 with a high density thick film interconnect 42. This circuit structure may, for example, be used in a system-on-a-package (SoP) structure for hearing instrument products or other products requiring high volumetric density for capacitors and other integrated passives (e.g., inductors, resistors) in radio frequency (RF), Bluetooth, and high-speed wireless (e.g., wideband) communication modules.

The ceramic substrate 40 is a machinable ceramic material, such as Al_2O_3 . Metal filled (e.g., Ni, Ag, Ag-Pd, W, etc.) through holes 54 are machined through the substrate 40 (e.g., laser drilled or green tape punched) to provide front to back electrical connections. As noted above, the machinable nature of ceramic enables the through holes 54 to be machined in a high density pattern. Bonding pads 52 on the bottom surface of the substrate 40 provide an electrical connection to the vias 54. The bonding pads 52 may be fabricated using copper, low temperature Ag, or some other suitable conductive material. The bottom surface of the substrate may be covered by a protective coating material 50, such as Si_3N_4 .

The high density thick film interconnect layers 42 are fabricated on the upper surface of the ceramic substrate 40, and provide substrate level routing and electrical connections between the thin film circuit and the bonding pads 52. Routing layers 56 and metal filled vias 58 in the HDI layers (stack) 42 may be fabricated using a photodefineable thick film dielectric material with high density conductive routing layers 56 (e.g. Au) or high temperature fired conductive materials (e.g., W, Mo. etc.). In addition, the HDI layers 42 may include buried resistors and inductors.

The buffer (smoothing) layer 44 is fabricated over the HDI interconnect layers 42 to provide a smooth surface for the MLC 48, as described above. The buffer layer 44 also provides a moisture barrier and additional electrical isolation between the HDI layers 42 and the thin film circuit layers. In addition, the buffer layer 44 may help to prevent outdiffusion of any volatile ions that could influence the electrical performance of the MLCs 48, and prevent oxidation of the conductive material in the contact holes 66 during high temperature processing of the ferroelectric thin films in the stack 48. The buffer layer 44 may, for example, be fabricated using a polished thick film material or by depositing a layer of fritted glass material with subsequent firing at high temperatures (fire polished), as described below with reference to Figures 7 and 8. As illustrated, the buffer layer 44 may also include

conductive material in the contact holes 66 to electrically connect the thin film circuit layers, including the MLC 48, with the HDI layer 42.

The MLC structure 48 is attached to the buffer layer 44 with an adhesion layer 46, such as TiOx and/or Al₂O₃. The illustrated example includes a four layer capacitor formed by depositing a BST dielectric material 62 sandwiched between conductive (e.g., Pt) electrode layers 60. Each of the four layers of the MLC structure 48 can have different properties and functions which may include different capacitance-voltage characteristics (tunabilities). The MLC structure 48 is a mesa-structure, which may be fabricated using photolithography based patterning techniques, as described below with reference to Figures 9A and 9B. Preferably, the capacitor formed from the top two conductive electrode layers 60 and the top-most dielectric layer 62 is a voltage variable (tunable) capacitor.

A first interlayer dielectric (ILD) 64 is fabricated over the MLC 48 and buffer layer 44. The dielectric 64 may, for example, be phosphosilicate glass (PSG) or some other suitable dielectric material. Contact holes 66 are etched in the first ILD 64, the buffer layer 44 and HDI interconnect layer stack 42 and filled with metal to provide an interconnect by contacting metal interconnect layer (M1) 67 to select electrode layers of the MLC 48 and to metal filled through holes 54. The interconnect layer (M1) 67 may, for example, be TiW/Al/TiW, TiW/Al, TiW/Pt/Au or TiW/Cu.

A second interlayer dielectric (ILD2) 68 is fabricated over the first ILD 64 and the interconnect (M1) 67. The ILD2 68 may, for example be PSG or some other suitable dielectric material, and includes metal filled vias 72 that provide a second interconnect (M2). The second interconnect layer (M2) 73 may, for example, be TiW/Au or TiW/Cu. In addition, the vias 72 may be coated with a nitride layer 70 prior to metalization in order to create one or more nitride capacitors (e.g., Si₃Ni₄) (C1). The illustrated nitride capacitor (C1)

is formed by depositing a nitride layer 70 between the two metal interconnect layers 67, 73 (M1 and M2).

Also illustrated is a thin film resistive layer 76 (R1) that is deposited over the second interlayer dielectric and is electrically connected in series with the nitride capacitor (C1) via the second interconnect (M2). The second interconnect 73 (M2) is covered with a protective coating 74 (e.g., Si_3N_4), and is connected to a front metal bump layer 78 (e.g., TiW/Au). The front metal bump layer 78 may, for example, be used to electrically connect the structure to an integrated circuit (IC) chip to form a system-on-a-package (SoP) structure.

Figures 5-9 illustrate example processes for fabricating the circuit structure of Figure 4. Figure 5 is a flow diagram illustrating the overall fabrication process. Figure 6 is a flow diagram illustrating an example process for fabricating the ceramic substrate and HDI routing and dielectric layers. Figure 7 illustrates an example process for fabricating the buffer (smoothing) layer on top of photodefineable thick film dielectric material with high density conductive routing layers 56. Figure 8 illustrates an example process for fabricating a patterned fritted glass smoothing layer. Figures 9A and 9B are a flow diagram illustrating an example process for fabricating the thin film circuit, including the MLC structure.

With reference first to Figure 5, the overall process for fabricating the example circuit structure of Figure 4 is illustrated as a five step process. In the first step 80, the core HDI substrate is fabricated. This includes the fabrication of the ceramic substrate with the HDI routing and dielectric layers. In the second step 82, the buffer (smoothing) layer is fabricated on the HDI substrate. In the third step 83, an adhesion layer is fabricated on top of the buffer (smoothing) layer. In the fourth and fifth steps 84, 86, the thin film circuit is fabricated by building the MLC structure on top of the buffer layer and integrating the MLC with additional thin film circuit components, such as additional high frequency capacitors, inductors, thin film resistors and/or other passive components.

With reference now to Figure 6, the example process for fabricating the ceramic substrate and HDI layers begins at step 90. At step 92, through holes are machined through the ceramic substrate material using a laser beam. In other examples, however, the through holes could be machined using other processes, such as a pneumatic abrasion, ultrasonic milling, green tape punching or other suitable method for machining high density through holes in ceramic. The through holes are then filled with metal at step 94. The process then proceeds to step 96 to fabricate the first HDI routing layer.

At step 96, a layer of conductive material (e.g., Au) is deposited on the ceramic substrate (e.g., by screen printing) to form the first routing layer. The routing layer is dried at step 98 and fired at step 100. Steps 96-100 may then be repeated to fabricate a thicker routing layer. Once a routing layer with the desired thickness has been deposited, the process proceeds to step 102 to pattern the routing layer.

At step 102, a photoresist material is deposited over the conductive material (e.g., by spinning) and is baked to cure the photoresist. A mask is then aligned over the photoresist layer and UV exposed at step 104 in order to pattern a negative image of the routing layout in the photoresist material. The patterned photoresist is developed and hard baked at step 106. The conductive material that is exposed through the photoresist is then wet etched at step 108 to pattern the routing layer, the photoresist is stripped, and the routing layer is cleaned. The process then proceeds to step 110 to deposit and pattern a dielectric layer over the routing layer.

A photosensitive (photodefineable) thick film dielectric material is deposited (e.g., by screen printing) over the HDI routing layer at step 110, and the deposited dielectric material is dried at step 112. A mask is then aligned over the photosensitive dielectric layer and UV exposed at step 114 in order to pattern vias for exposing select portions of the HDI routing layer. At step 116, the UV exposed dielectric is developed, rinsed and dried, forming through

holes in the HDI dielectric layer. The structure is then fired at step 118. If another HDI routing layer is required, then the process returns to step 96. Else, the process ends at step 122.

In another example, a non-photosensitive thick film material could be used to form the HDI dielectric layers by UV exposing a photoresist material and etching the thick film material to form the through holes.

Figure 7 illustrates an example process for fabricating the buffer (smoothing) layer using a thick film material. The process begins at step 130 after the core HDI substrate has been fabricated. At step 132 a photosensitive thick film dielectric paste is deposited (e.g., by screen printing) on top of the HDI layers. In other examples that do not include a HDI layer (e.g., Figure 1), the thick film dielectric paste may be deposited directly on the ceramic substrate. The thick film paste is then dried (e.g., at 120°C for about 15 minutes) at step 134 to remove volative organic vehicles.

At step 136 the layer of thick film dielectric material is UV exposed. The photosensitive thick film is then developed, rinsed and dried at step 138. The thick film material is then hardened by firing (e.g., peak of 850°C for about 10 minutes) at step 140. Steps 132-140 may then be repeated one or more times to achieve a desired thickness for the buffer layer. Once the thick film material has been fabricated to a desired thickness, the top surface of the buffer layer is polished to create a smooth surface. The surface of the buffer layer may, for example, be polished to have a final surface roughness (Ra) of about 0.06 to about 0.08 μm .

In another example, a non-photosensitive thick film material could be used by UV exposing a photoresist material and etching the thick film material to form the vias and/or through holes.

Figure 8 illustrates an example process for fabricating the buffer (smoothing) layer using a fritted glass material. The process begins at step 160 after the core ceramic substrate containing HDI routing layers (or without HDI routing layers) has been fabricated. At step 162 a thick film glass material with organic binders is patterned (e.g., by screen printing) on the HDI layers, leaving the non-filled through holes exposed. The fritted glass material may, for example, be deposited to a thickness of about 20um to about 25um. The fritted glass material is then dried to remove volative organic binders at step 164 and is fired (e.g., peak of 1250° C) at step 166. Steps 162-166 may be repeated, as needed, in order to provide a smoother surface. After firing, the formed glass buffer layer provides a smooth surface for fabricating the MLC or other thin film passives.

After the buffer layer has been fabricated, the process proceeds to step 168 to fill the through holes. At step 168, a metal paste (e.g., Ni) is deposited in the through holes. The metal paste is then dried at step 170 and fired at step 172. The metal paste should be fired at a temperature lower than the glass buffer layer firing temperature (e.g. about 1000 to about 1100° C). Steps 168-172 may then be repeated to ensure that the through holes are completely filled. Once the through holes in the buffer layer have been filled with metal, the process ends at step 174.

With reference to Figures 9A and 9B, the example process for fabricating the thin film circuit begins by cleaning the surface of the buffer (smoothing) layer at step 180. At step 182 an adhesion layer (e.g., TiOx) is deposited over the buffer (smoothing) layer. The first electrode layer (e.g., Pt) of the MLC structure is then deposited over the adhesion layer at step 184 and the structure is annealed to stabilize the electrode layer at step 186. A high or low permittivity dielectric layer is then deposited over the first electrode layer at step 188. The dielectric layer may, for example, be deposited by chemical solution deposition, physical vapor deposition, chemical vapor deposition or by other suitable means. In the case of a

tunable capacitor, a high permittivity dielectric layer 62 is used (e.g., BST material). The dielectric layer is then annealed at step 190, and a second electrode layer is deposited over the dielectric at step 192 forming a parallel plate capacitor. Steps 188-192 may then be repeated to create additional capacitor layers.

At steps 194 and 196, the layers of electrode and dielectric materials are patterned and ion milled to form a mesa-structure, as illustrated in Figure 4. Selected exposed dielectric layers are then patterned and etched at step 198 to create vias exposing the underlying electrode layers. Any damage to the dielectric layers caused by the etching step 198 is then repaired by annealing at step 200.

At step 202 a first interlayer dielectric (ILD1) is deposited over the MLC and buffer (smoothing) layers. The interlayer dielectric may, for example, be a PSG material. Through holes (vias) are then patterned and etched through the interlayer dielectric at steps 204 and 206 to expose the vias in the buffer layer and MLC. At step 208 the structure is annealed to repair any damage to the high permittivity dielectric layers of the MLC structure caused by the etching steps. Then, at step 210 a metallic material, such as TiW/Al/TiW, TiW/Al, TiW/Pt/Au or TiW/Cu, is deposited, patterned and etched to provide an interconnect (M1) to the MLC and HDI routing layers via the contact holes.

At step 212 a second interlayer dielectric (ILD2) is deposited over the first interlayer dielectric (ILD1) and the interconnect layer (M1). The second interlayer dielectric may, for example, be a PSG material. Then, at step 214 a thin film resistive layer is deposited on the ILD2. Other thin film components may also be patterned on the ILD2 at this stage in the process. Then, at step 216 vias are patterned and etched through the ILD2 to access the interconnect layer (M1).

At step 218 an intermediate permittivity dielectric material is deposited in the through holes of the ILD2 layer to provide a dielectric layer for one or more low/intermediate

permittivity dielectric capacitors (e.g., Si_3N_4 , etc.). The dielectric material is then patterned and etched at step 220 to provide connections to the interconnect layer (M1) where needed. At step 222, a metallic material, such as TiW/Au or TiW/Cu, is deposited on the ILD2 layer and in the vias of the ILD2 layer to provide an interconnect (M2) to the filled contact holes in the first ILD layer (ILD1), and also to create low/intermediate permittivity dielectric capacitors (C1). The interconnect layer (M2) is then patterned and plated at step 224 to create interconnects and connections to the thin film components above the ILD2 layer. High frequency inductors may also be formed and interconnected at this stage in the process. Then, a seed layer is patterned and etched at step 226 and the final plated metal layer is dehydrated at step 228. The metal interconnects (M2) may then be covered with a protective layer, such as a Si_3N_4 overcoat, at step 230.

At step 232, any protective layer on the back side of the ceramic substrate is removed and the back side of the ceramic wafer is polished to access the metal filled through holes. A conductive seed layer is then deposited, patterned, plated and etched on the back side of the ceramic substrate at steps 234 and 236 to form bonding pads. The bonding pads may, for example, be fabricated using a TiW/Cu seed layer and a Cu plating.

At step 238, the protective overcoat on the top layer of the structure is patterned and etched to expose select portions of the interconnect layer (M2). A metal bump layer (e.g., TiW/Au) may then be deposited and etched at steps 240 and 242 to form bonding pads on the top surface of the structure. The top layer bonding pads may, for example, be used to connect with the bonding pads of an integrated circuit, forming a SoP structure.

This written description uses examples to disclose the invention, including the best mode, and also to enable a person skilled in the art to make and use the invention. It should be understood that the examples depicted in the Figures may not be drawn to scale. The

patentable scope of the invention may include other examples that occur to those skilled in the art.

It is claimed:

1. A thin film integrated circuit, comprising:

a ceramic substrate;

a thin film multi-level capacitor (MLC) that includes at least one high permittivity dielectric layer between at least two electrode layers, the electrode layers being formed from a conductive thin film material; and

a buffer layer between the ceramic substrate and the thin film MLC, the buffer layer having a smooth surface with a surface roughness (Ra) less than or equal to 0.08 micrometers (μm);

wherein the thin film MLC is fabricated on the smooth surface of the buffer layer.

2. The thin film integrated circuit of claim 1, wherein the surface roughness (Ra) of the buffer layer is less than or equal to 0.06 micrometers (μm).

3. The thin film integrated circuit of claim 1, wherein the surface roughness (Ra) of the buffer layer is less than or equal to 0.03 micrometers (μm).

4. The thin film integrated circuit of claim 1, wherein the MLC is a tunable capacitor.

5. The thin film integrated circuit of claim 4, wherein the high permittivity dielectric layer is a compound containing Barium Strontium Titanium Oxide.

6. The thin film integrated circuit of claim 1, wherein the ceramic substrate is Al_2O_3 .

7. The thin film integrated circuit of claim 1, wherein the ceramic substrate is AlN.

8. The thin film integrated circuit of claim 1, wherein the ceramic substrate is Mg_2SiO_4 .
9. The thin film integrated circuit of claim 1, wherein the ceramic substrate is MgTiO_3 .
10. The thin film integrated circuit of claim 1, wherein the MLC has an overall capacitance density of about $10 \text{ fF}/\mu\text{m}^2$ to about $390 \text{ fF}/\mu\text{m}^2$.
11. The thin film integrated circuit of claim 1, wherein the buffer layer is a polished thick film dielectric material.
12. The thin film integrated circuit of claim 1, wherein the buffer layer is a fritted glass dielectric material.
13. The thin film integrated circuit of claim 12, wherein the ceramic substrate includes through holes filled with conductive material and wherein a surface of the ceramic substrate is completely covered by the fritted glass dielectric material.
14. The thin film integrated circuit of claim 12, wherein the ceramic substrate includes through holes filled with conductive material and wherein a surface of the ceramic substrate is partially covered by fritted glass dielectric material, leaving the through holes uncovered.
15. The thin film integrated circuit of claim 1, further comprising:
 - a high density interconnect (HDI) layer between the ceramic substrate and the buffer layer.

16. The thin film integrated circuit of claim 15, wherein the HDI layer including at least one routing layer and at least one layer of a thick film dielectric material.
17. The thin film integrated circuit of claim 15, wherein the HDI layer further includes one or more metal filled vias to electrically connect the MLC to metal filled through holes in the ceramic substrate.
18. The thin film integrated circuit of claim 15, wherein the HDI layer includes one or more buried passive circuit components.
19. The thin film integrated circuit of claim 1, further comprising:
 - one or more additional passive thin film devices coupled to the MLC.
20. The thin film integrated circuit of claim 1, further comprising:
 - an adhesion layer between the buffer layer and the MLC.
21. The thin film integrated circuit of claim 20, wherein the adhesion layer includes one or more layers of thin film TiOx.
22. The thin film integrated circuit of claim 20, wherein the adhesion layer includes one or more layers of thin film Al₂O₃.
23. The thin film integrated circuit of claim 1, wherein the thin film integrated circuit is attached to an integrated circuit chip to form a system-on-a-package (SoP) structure.

24. A method of manufacturing a thin film integrated circuit on a ceramic based substrate, comprising:

depositing a buffer layer over the ceramic based substrate, the buffer layer having a smooth surface with a surface roughness (Ra) less than or equal to 0.08 micrometers (μm);

depositing an adhesion layer over the smooth surface of the buffer layer;

depositing a first thin film electrode layer over the adhesion layer;

depositing a high permittivity dielectric layer over the first thin film electrode layer;

and

depositing a second thin film electrode layer of the high permittivity dielectric layer;

wherein the first thin film electrode layer, high permittivity dielectric layer and second thin film electrode layer form a thin film multi-level capacitor (MLC) structure.

25. The method of claim 24, wherein the surface roughness (Ra) of the buffer layer is less than or equal to 0.06 micrometers (μm).

26. The method of claim 24, wherein the surface roughness (Ra) of the buffer layer is less than or equal to 0.03 micrometers (μm).

27. The method of claim 24, further comprising:

depositing one or more high permittivity dielectric layer and one or more additional thin film electrode layers over the second thin film electrode layer to form additional capacitors in the MLC structure.

28. The method of claim 24, further comprising:

fabricating a high density interconnect (HDI) layer on a ceramic substrate to form the ceramic based substrate.

29. The method of claim 24, further comprising:

depositing an interlayer dielectric layer over the buffer layer and the MLC;

fabricating one or more additional passive thin film devices on the interlayer dielectric layer; and

depositing an interconnect layer to electrically couple the one or more additional passive thin film devices to the MLC.

30. The method of claim 24, wherein the high permittivity dielectric layer is a compound containing Barium Strontium Titanium Oxide, forming a tunable MLC.

31. The method of claim 24, wherein the ceramic based substrate includes a layer of Al_2O_3 .

32. The method of claim 24, wherein the ceramic based substrate includes a layer of AlN .

33. The method of claim 24, wherein the ceramic based substrate includes a layer of Mg_2SiO_4 .

34. The method of claim 24, wherein the ceramic based substrate includes a layer of MgTiO_3 .

35. The method of claim 24, wherein the MLC has an overall capacitance density of about $10 \text{ fF}/\mu\text{m}^2$ to about $390 \text{ fF}/\mu\text{m}^2$.

36. The method of claim 24, wherein the step of depositing a buffer layer comprises:
- depositing one or more layers of thick film material over the ceramic based substrate;
- and
- polishing a top surface of the thick film material to create the smooth surface.
37. The method of claim 24, wherein the step of depositing a buffer layer comprises:
- depositing a glass dielectric material over the ceramic based substrate.

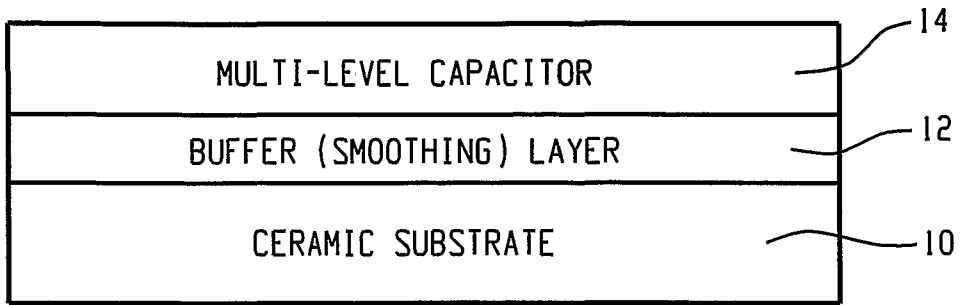


Fig. 1

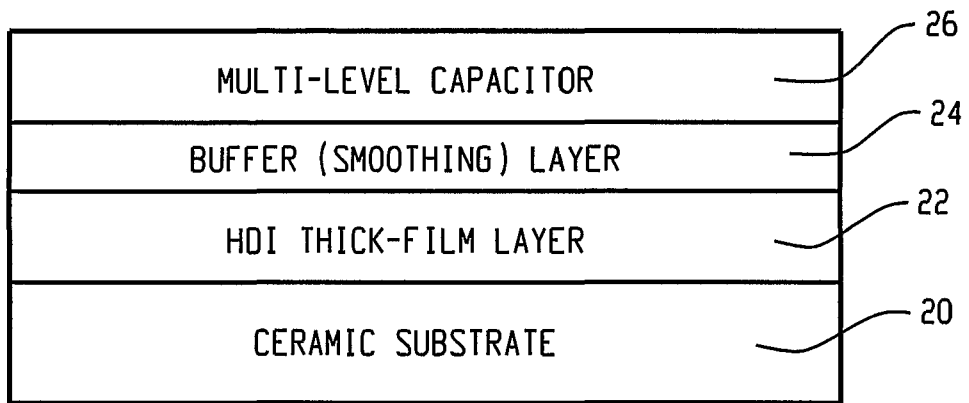


Fig. 2



Fig. 3

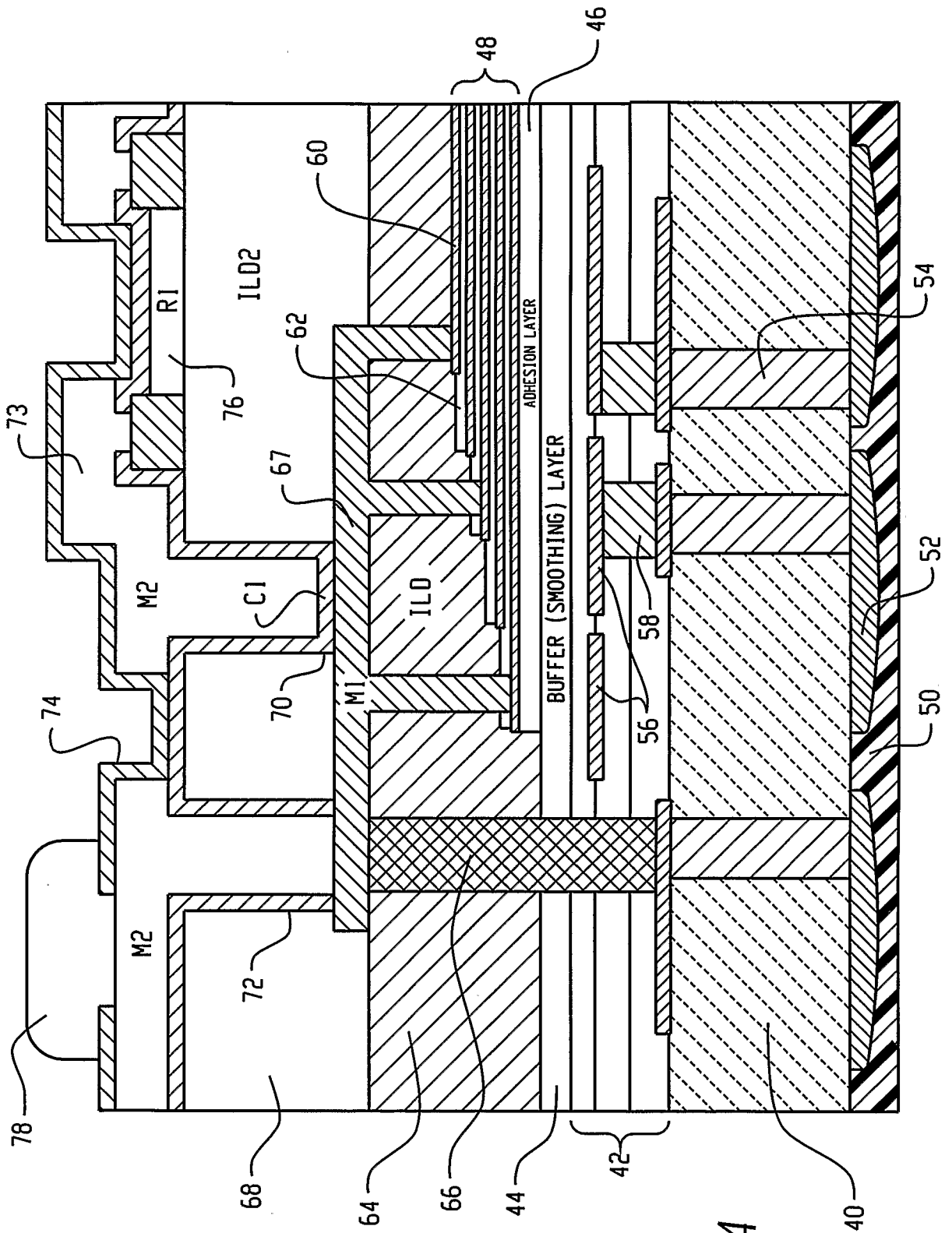


Fig. 4

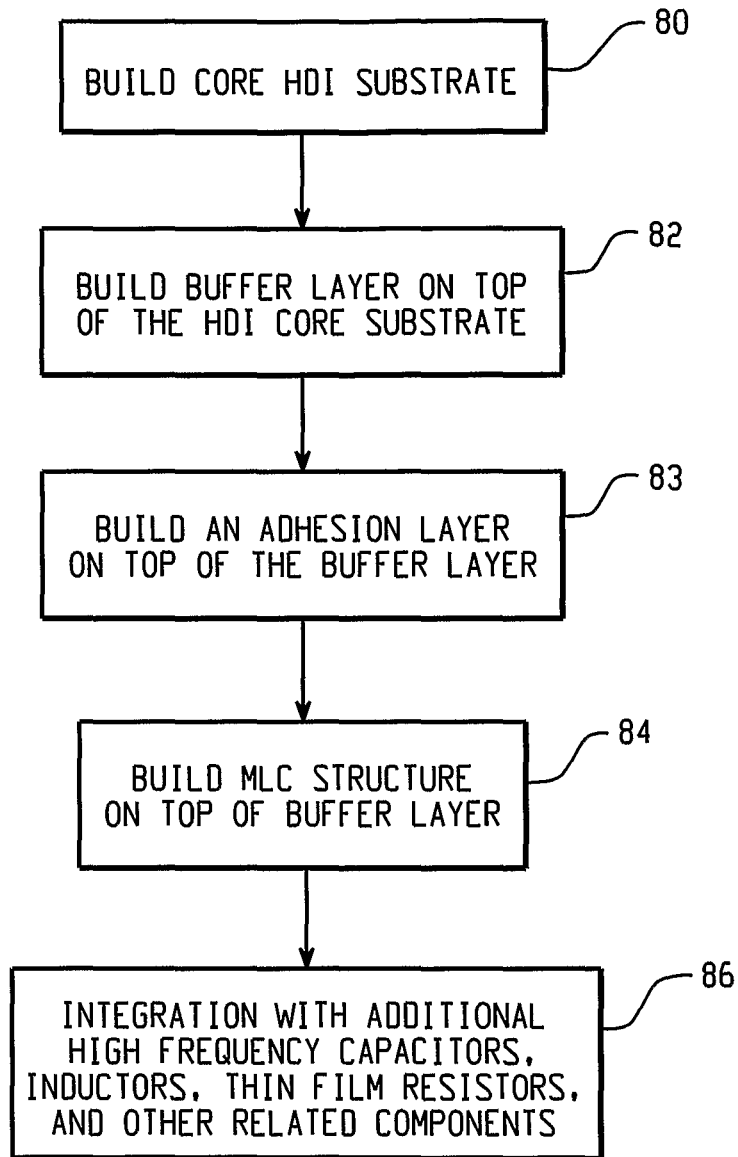


Fig. 5

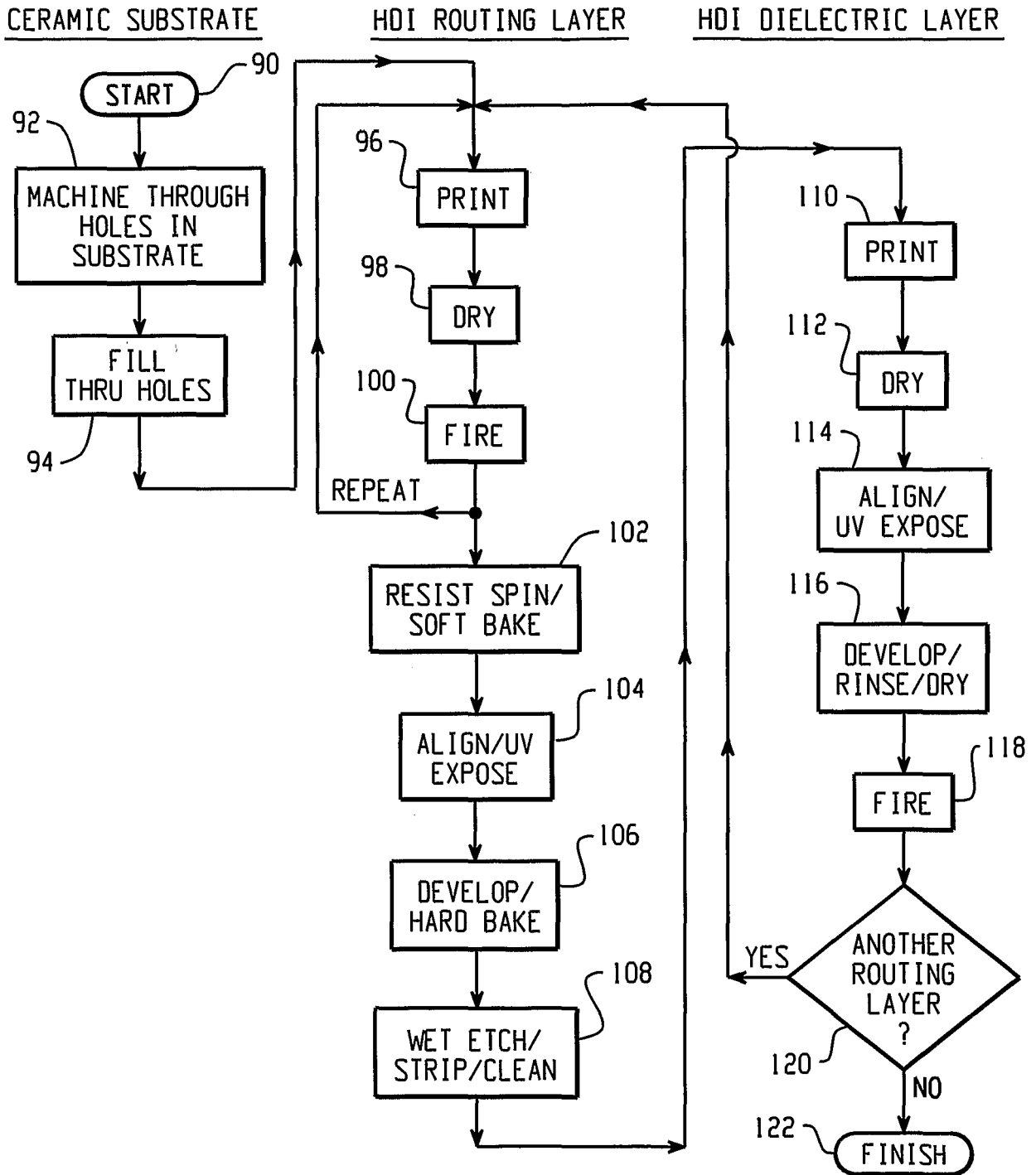


Fig. 6

BUFFER (SMOOTHING) LAYER

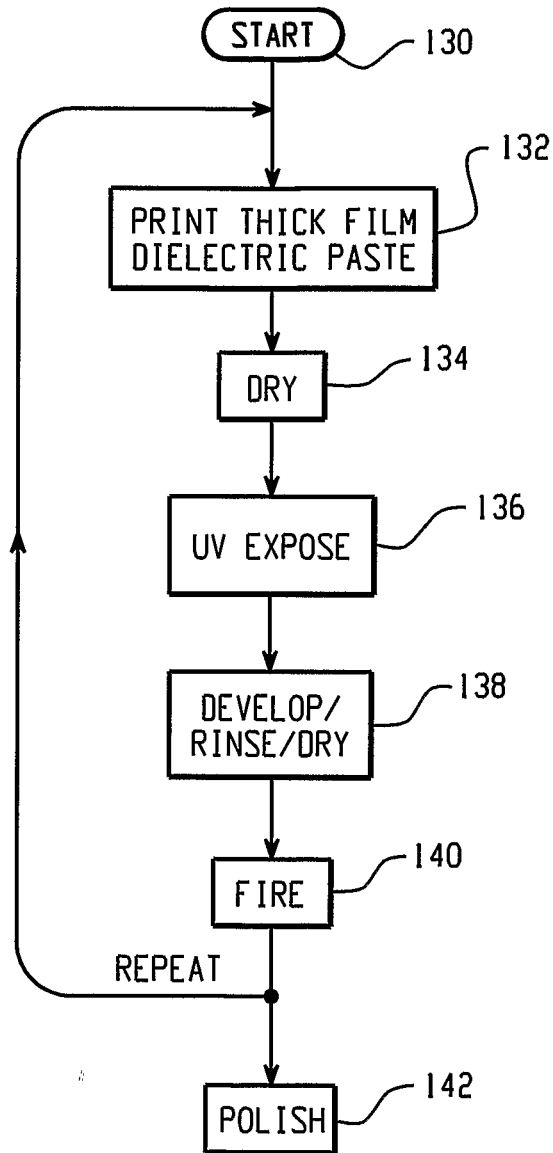


Fig. 7

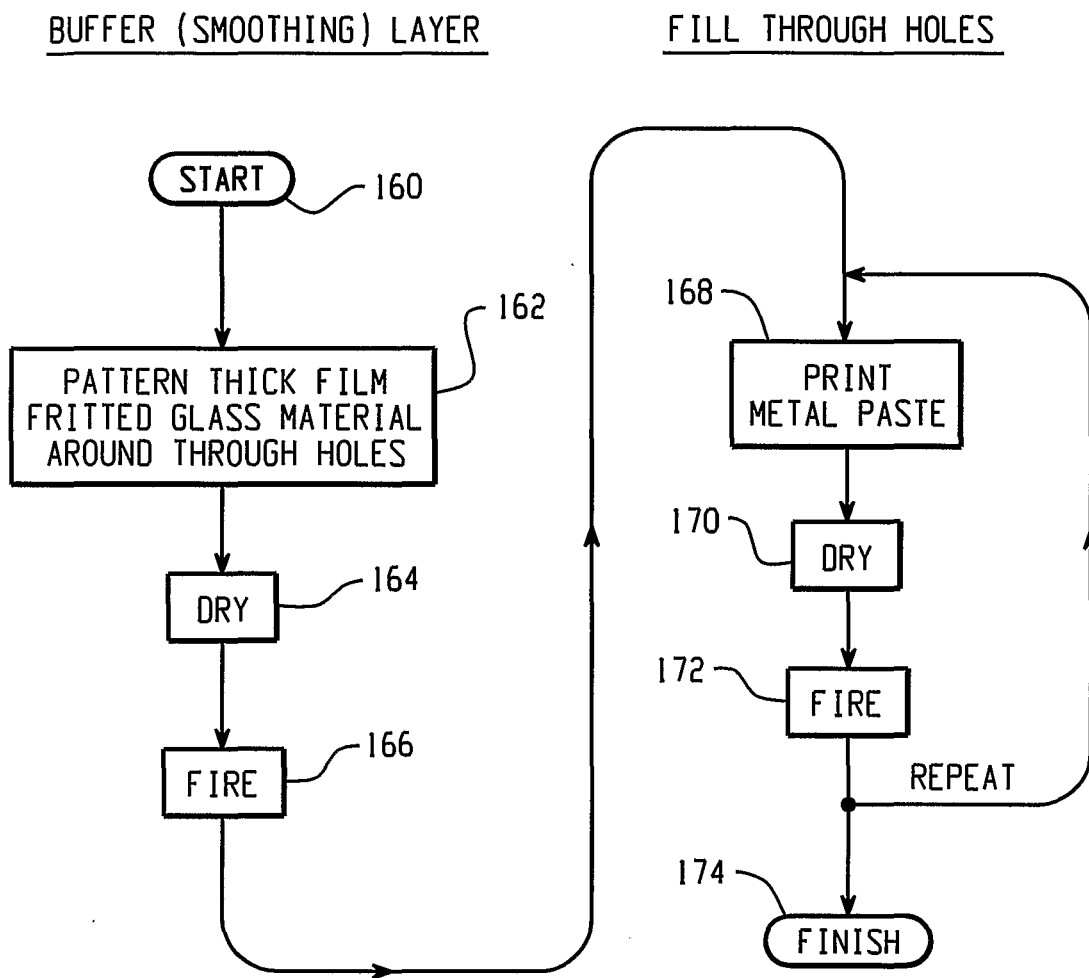


Fig. 8

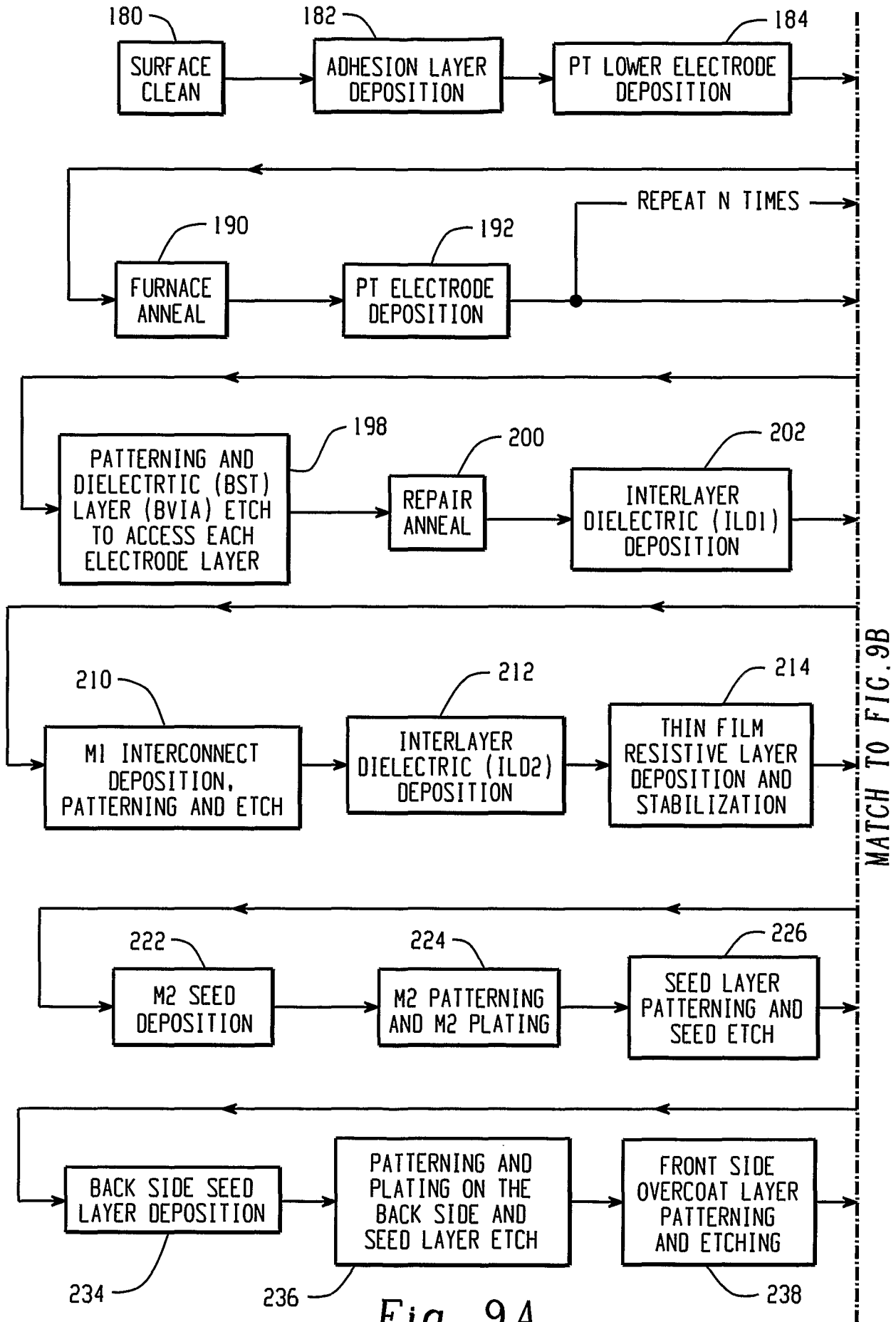


Fig. 9A

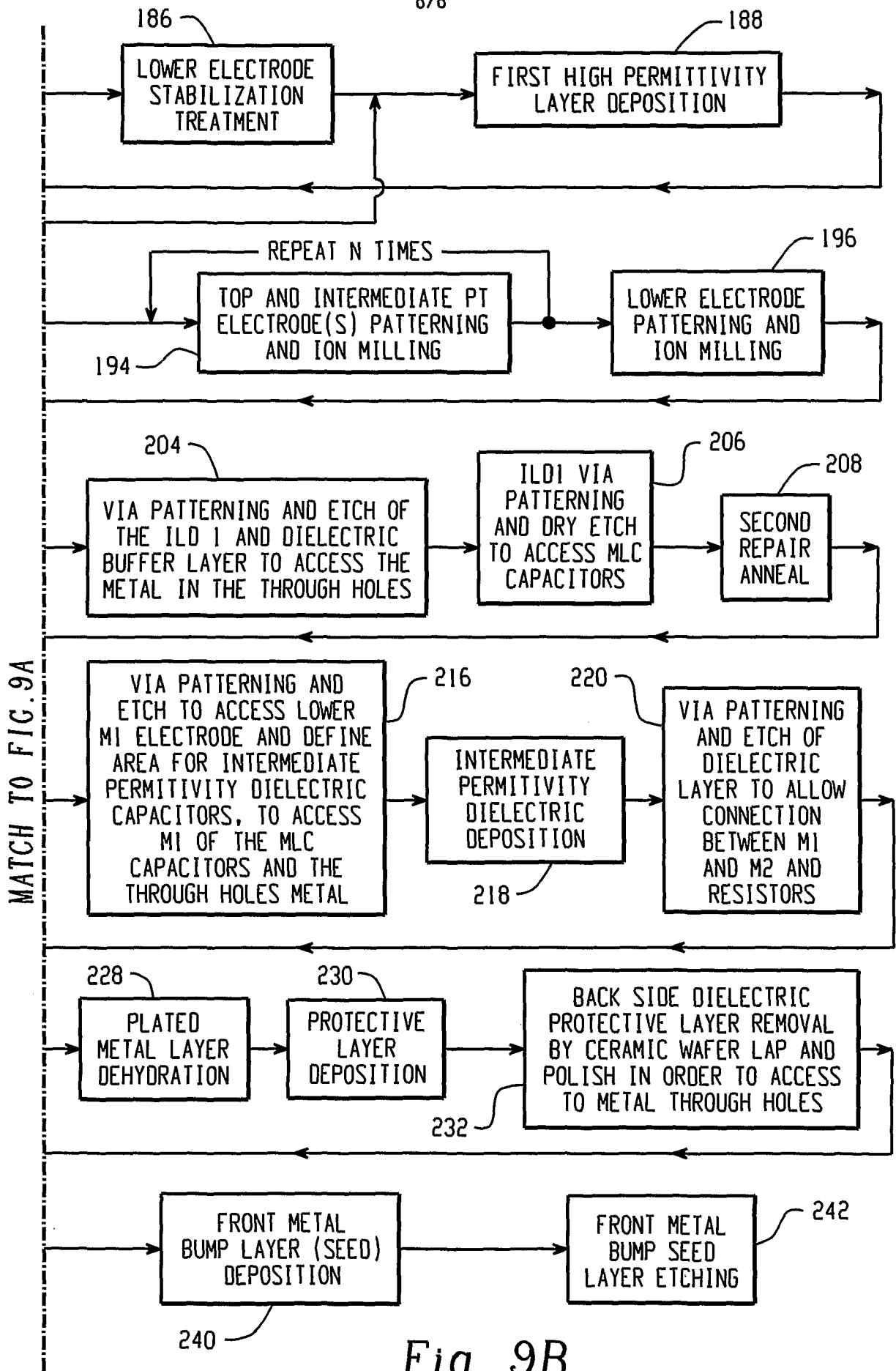


Fig. 9B

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CA2004/002053

A. CLASSIFICATION OF SUBJECT MATTER IPC 7 H01L-27/00, H01L-21/77, H01G-4/33

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L-27/00, H01L-21/77, H01G-4/33

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base, and, where practicable, search terms used)
Canadian Patent Database, Pluspat, Delphion, IEEE xplore
keywords: ceramic, substrate, buffer, layer+, capacitor, smooth+, polish+, rough+, thin film

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	JP 2001-223301 (Horikoshi et al) 17 August 2001 (17-08-2001) (abstract, par [0012], [0017] of the computer translation)	1-10, 20, 23-27, 30-37
Y	JP 2000-323845 (Hiwatari) 24 November 2000 (24-11-2000) (abstract, par [0010] to [0014] of the computer translation)	1-12, 20, 23, 37
Y	JP 61-145856 (Kudo et al) 3 July 1986 (03-07-1986) (abstract)	1-3, 24-26, 36

Further documents are listed in the continuation of Box C.

Patent family members are listed in annex.

*" Special categories of cited documents :	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A" document defining the general state of the art which is not considered to be of particular relevance	"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E" earlier application or patent but published on or after the international filing date	"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&" document member of the same patent family
"O" document referring to an oral disclosure, use, exhibition or other means	
"P" document published prior to the international filing date but later than the priority date claimed	

Date of the actual completion of the international-type search
19 January 2005 (19-01-2005)Date of mailing of the international-type search report
10 March 2005 (10-03-2005)Name and mailing address of the ISA/CA
Commissioner of Patents
Canadian Patent Office - PCT
Ottawa/Gatineau K1A 0C9
Facsimile No. 1-819-953-9358Authorized officer
Leah Smith (819) 956-9966

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CA2004/002053

Patent Document Cited in Search Report	Publication Date	Patent Family Member(s)	Publication Date
JP2001223301	17-08-2001	JP2001223301 A	17-08-2001
JP2000323845	24-11-2000	JP2000323845 A	24-11-2000
JP61145856	03-07-1986	JP61145856 A	03-07-1986