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特別解説

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Review on Ferroelectric Thin Film Devices: Fundamental Aspects and Integration Challenges

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Abstract

This review on perovskite (ABO_3) materials focuses primarily on ferroelectric films used in devices for charge storage such as $Pb(Zr,Ti)O_3$ (PZT) for non-volatile ferroelectric random access memory (FeRAM) and high dielectric constant materials containing $(Ba,Sr)TiO_3$ (BST), but it also emphasizes general principles on the integration of electroceramics in devices and microelectro mechanical systems (MEMS). The number of papers reported in the literature on ferroelectrics has expanded greatly in the past 20 years, but classical reliability problems in ferroelectric devices remain. Greater emphasis is needed on understanding key mechanisms which result in degradation of ferroelectric materials' electrical characteristics in devices over time and with usage particularly between the ferroelectric film and electrode interface. In addition, better quantification of numerical measures of thin films are needed in order to more closely relate the process conditions to the materials characteristics and the resultant electrical properties. Furthermore, materials reliability and analysis of complex systems is a topic that needs further consideration when researching/working with ferroelectric devices. Finally, problems with materials reliability in ferroelectric devices are in need of further detailed investigation by researching and understanding the mechanisms which are the root causes of ferroelectric polarization losses in actual devices.

1. Introduction

Perovskite based materials have the chemical formula ABO_3 where A and B are different cations that includes many different types of materials with a wide variety of properties. In most cases, perovskites are oxides, but there are exceptions such as halide and hydride perovskites (ABX_3, X = F, Cl, Br, I and H). Examples of perovskite materials and their properties are shown in Table 1.

Of the perovskites, ferroelectric and piezoelectric materials are highly functional because of their wide ranging properties due to the perovskite crystal lattice[1-3]. Of these materials, ferroelectrics are widely known and exhibit a spontaneous electrical polarization that can be reversed by the application of an external electric field where the polarization value is a function of temperature. Piezoelectric materials generate an electric field or electric potential in response to applied mechanical stress. The key point of utilizing these materials effectively is maintaining the crystal structure while processing the material in various forms such as thin films (<500nm) thick film (>500nm) or in ceramic or bulk form needed for microelectro mechanical systems (MEMS) or in semiconductor devices. In the case of thin films where the materials are deposited on a substrate, the crystallographic orientation is important since ferroelectric materials are anisotropic. When these materials are put in a capacitor or parallel plate type structure with electrodes on a substrate and integrated further into electronics wide ranging electro-mechanical devices are possible such as piezo-MEMS[4]. In addition, certain classes of perovskites also exhibit electro caloric properties[5]. Therefore, utilizing these materials in energy scavenging/harvesting[6] as well as in photocatalytic hydrolysis applications is a topic of intense research[7].

1.1 Ferroelectric film challenges

In general, from reviewing the ferroelectric film and related device literature there has been considerable

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Table 1　Examples of Perovskite materials and their properties

Physical Property	Compound examples
Insulator	$LaAlO_3$, $LaGaO_3$, $NdGaO_3$, $LaCrO_3$, $LaFeO_3$
Paraelectricity, High-K dielectric	$SrTiO_3$, $(Ba_{1-x}Sr_x)TiO_3$, $(Pb_{1-x}La_x)TiO_3$, $Ba_2EuZrO_{5.5}$, $CaCu_3Ti_4O_{12}$
Semiconductivity	$LaMnO_3$, $(La_{1-x}Ca_x)MnO_3$, $PbCrO_3$, $LaTiO_3$, $SrPbO_3$, $LaFeO_3$(p-type)
Half Metallicity	$LaBaMn_2O_{5.5}$, $YBaMn_2O_{5.5}$, Sr_2FeMoO_6, Ba_2FeMoO_6, Ca_2FeReO_6
Metallic conductivity	$LaNiO_3$
Pauli Paramagnetic Metallicity	$SrMoO_3$, $LaNiO_3$, $SrCrO_3$
Pauli Ferromagnetic Metallicity	$SrRuO_3$, Sr_2FeMoO_6
Ferromagneticity	$LaMnO_{3.15}$, $(La_{1-x}Ca_x)MnO_3$, $(Sr_{1-x}La_x)MnO_3$
Antifferomagneticity	$BiMnO_3$, $LaFeO_3$, $LaMnO_3$, $NaOsO_3$
Colossal magnetoresistance	$Sr_{0.3}La_{0.7}MnO_3$
Multiferroicity	$BiFeO_3$, $BiMnO_3$
Antiferroelectricity	$PbZrO_3$, $NaNbO_3$
Ferroelasticity	$LaCoO_3$, $CaTiO_3$
Piezoelectricity	$Pb(Zr_{1-x}Ti_x)O_3$, $(K,Na)NbO_3$
Magnetoelasticity	$Sr_2(Fe_{1-x}Cr_x)ReO_6$
Spin glass	$CaRuO_3$, Sr_2FeMoO_6
Mott Insulator	$LaTiO_3$, $YTiO_3$
Superconductivity	$(Ba_{0.6}K_{0.4})BiO_3$, $YBa_2Cu_3O_7$, $Bi_2Sr_2Ca_2Cu_3O_{10-\delta}$, $MgCNi_3$
Ionic conductivity	$BaCeO_3$, $BaCe_{1-x}Y_xO_{3-\delta}$, $(Sm_{1-x}Ca_x)AlO_{3-x/2}$
Hydrogen storage materials	$NaMgH_3$
Pigment materials	$YAl_{1-x}Cr_xO_3$, $Sr(Sn_{0.6}Ln_{0.4})O_3$
Catalyst	$La_{3.5}Ru_{4.0}O_{13}$, $(La_{1-x}Ce_x)CoO_{3+\delta}$

growth in ferroelectric film research based upon the number of publications (Fig. 1)[8]. A large part of this growth in research was driven by extending applications for high K dielectrics and ferroelectric memories. Recently, the trend has leveled off due to growing emphasis world-wide on energy related research.

There are basically several key issues to consider with regards to ferroelectric materials in electroceramic devices such as 1) what is the relationship between the material and the desired electrical characteristics, 2) understanding and optimizing the processing conditions to obtain the desired electrical characteristics, 3) successfully harnessing the electrical/mechanical characteristics in a device and 4) how to maintain the desired electro-mechanical characteristics of the material with usage over time (reliability). The issues relating the electrical characteristics to theoretical models and mechanism has been a topic of much debate for many years and will likely continue due to the fact that processing conditions have a large impact on the electrical characteristics and separating the effects of the process, intrinsic effects, materials composition and device integration impact remain a challenge. For corporate engineers and researchers in general, the real challenge with these materials is trying to understand the complexity of the material-electrical characteristics interaction in enough detail to interpret one's own data in order to disseminate the real signal from extrinsic effects. The difficulty in determining what is the measurement signal depends a great deal on the measurement conditions and measurement know-how[9].

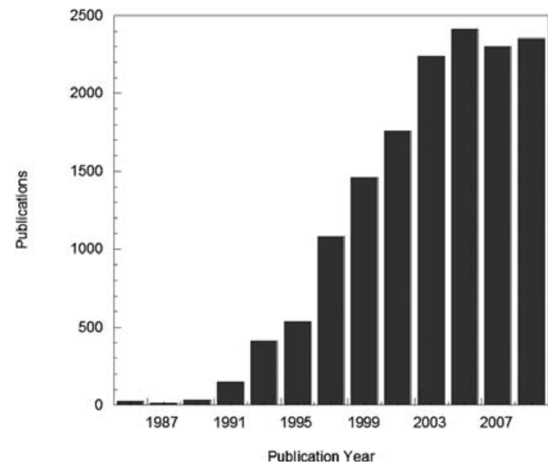

Fig. 1　Number of publications in the Web of Science database with "ferroelectric" and "film" as keywords excluding "multiferro" and "polymer" for two years intervals from 1985 to 2009.

One of the key reasons why it is difficult to relate process impact to the electrical properties is that although materials characterization techniques are very good and accurate for bulk properties characterization of films is more challenging. For example, in order to utilize the perovskite material it must be crystalline and standards are available for calibrating X-ray diffraction (XRD) equipment[10] which is used for measuring film crystallinity. However, there is no standardized set of characteristic principles or numerical values one can assign to a processed film with a particular composition

and thickness to access/grade the material's crystallinity numerically. In addition, distortion in the film lattice parameters due residual stress from the substrate must be considered. In order to compare one's results with someone else's results in the literature it is common to report XRD intensity in counts/s but for thin films it would be more instructive to report crystallinity as a function thickness such as counts/s/nm or a similar parameter to standardize the XRD peak intensities. Reporting intensities in a more standardized or normalized manner would allow for easy comparison and comparison with simulated values[11].

Another key issue is accessing the interface quality between the electrode and the ferroelectric material and then relating the interface to a capacitor or device electrical characteristics[12]. Currently this is no numerical scale that one can assign to quantify the quality of an interface in order to compare it with published work in the literature. Typically, the quality of the interface is accessed based upon electrical measurements such as the inverse capacitance extrapolated to zero thickness[13]. Recently, transmission electron microscopy (TEM) has made tremendous progress and resolution at the atomic level is now possible[14-15]. TEM provides tremendous information on the samples interface but it is basically a two dimension slice or image but the interface is three dimensional. As a result of difficulties in characterizing films and interfaces, ferroelectric materials development has progressed primarily empirically and processing is a mixture of art and science. First principles calculations or simulations of materials lattice by minimizing free energy using various simulation software modules has provided greater insight in linking the art of thin film processing to the theoretical predictions based upon scientific principles[16-17]. However, simulated prediction of material properties based upon first principles calculations capability is still limited. So the impact of film defects, impurities, compositional non-uniformity, oxygen non-stoichiometry, near surface crystalline-to-amorphous transformation (amorphization) etc,. which often occurs during device processing steps, and device related stresses cannot yet be easily input in to the initial boundary conditions needed for simulation, therefore there is a gap between actual devices and defect-free simulation results.

Processing of a ferroelectric film into a device is typically done using standard thin film fabrication techniques such as physical vapor deposition (PVD), i.e., radio frequency (RF) magnetron sputtering, chemical solution deposition (CSD or sol-gel) or chemical vapor deposition (CVD). Further processing steps are required to prepare a capacitor such as photolithograph, ultra-violet (UV) light exposure and plasma etching with corrosive gases containing F or Cl free radicals. These types of processing also damages the film crystal structure similar to plasma-induced damage of the ferroelectric materials during Ar ion-milling, ion beam etching (IBE), or during conventional reactive ion etching (RIE)[18-21]. In addition, hydrogen-induced damage may occur when the films are covered by H containing SiO_2 layers used to separate the metallization lines for connecting the device to the peripheral circuitry. These SiO_2 layers typically contain OH groups in low concentrations but in close proximity to the capacitor. They must be separated by encapsulation layers such Al_2O_3 or SiN_x prior to back end processing and before hermetic-passivation of the devices, etc.[22-23].

1.2 FeRAM

1.2.1 FeRAM market and technology

Taking ferroelectric random access memory (FeRAM) as an example, it has been in mass production for over 18 years and its characteristic and technical challenges have been documented in the literature[24-25]. Although it was originally thought that the FeRAM non-volatile memory would grow into a billion $ market per year similar to Flash due mobile digital products, it has to yet to achieve this level. Actually, the FeRAM market size is estimated to be in the hundreds of millions of dollars per year based corporate press releases. Japanese manufacturers such as Panasonic and Fujitsu Ltd. have dominant positions in manufacturing FeRAM, although Texas Instruments and Ramtron International Corp. also have manufacturing capabilities. The most recent version of the International Technical Roadmap for Semiconductors (ITRS) 2009 highlights the current characteristics of FeRAM[26] and what technical challenges lie ahead. Technology of FeRAM is scheduled to advance in 4 year cycles which is longer than other

types of memory technologies[26]. The technical challenges for FeRAM are how to increase the density which is related to the capacitor lateral size, decrease the operating voltage, and how thin a ferroelectric film capacitor can maintain device operating characteristics for 10 years over a range of temperatures as well as maintain high endurance to repeated cycling of reading/writing voltage pulses. Scaling issues refer to the both the film thickness, capacitor lateral dimensions and operating voltage and are clearly shown in Fig. 2. The figure indicates that the film thicknesses will have to be reduced further since this is the only way to decrease the operating voltage while maintain the same electric field strength in the ferroelectric capacitor. However, a number of research groups have pointed out that as the film decreases the voltage (electric field) needed to switching the ferroelectric domains in the capacitor increases exponentially for very thin films, i.e, < 30nm thick[27]. Further work is needed on this topic to better understand how to engineer a very thin ferroelectric film containing capacitor to retain charge in a non-volatile device at low voltage.

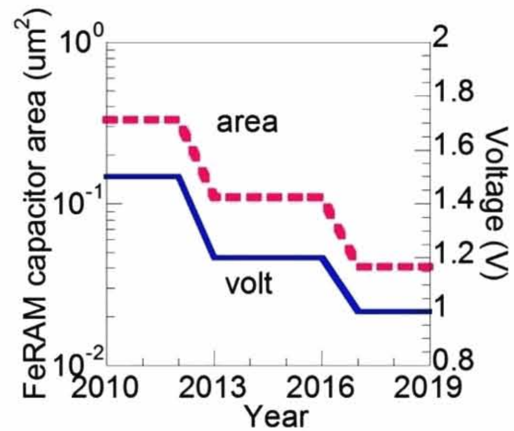

Fig. 2 FeRAM ITRS roadmap trends regarding operation voltage and capacitor area [26]. (© 2009, 2010 International Technology Roadmap for Semiconductors)

1.2.2 FeRAM new materials

More recently the academic community and industry has been exploring $BiFeO_3$ based thin film materials for future FeRAM capacitors because its higher net polarization due its higher Curie temperature and the fact that it does not contain lead[28]. Although $BiFeO_3$ films show high polarization, it does not appear that this material is yet suitable for devices because it is difficult to control the leakage current since the leakage conduction appears to be related to conduction thorough the ferroelectric domain walls[29-30]. To effectively utilize a material in a device, one of the most important thing is to reduce the system complexity and obtain the desired properties by optimizing the process conditions. So far optimum processing conditions have yet to be reported for $BiFeO_3$(BF), which allows for the capacitor high leakage current to be controlled.

Another way to try to effectively use BF in ferroelectric applications is to co-dope Bi and Fe in PZT[31]. The idea is to use the PZT matrix which has lower leakage and a perovskite lattice as a host. Recent results have shown that it is also possible to prepare capacitors of this material with $IrO_2/SrRuO_3$ as the top electrode and Pt as the bottom electrode[32]. Following this same approach Bi and Zn co-doping in PZT capacitors has also shown higher polarization and improved reliability[33]. Experimentally doping dipole pairs into the Bi based perovskite material has also show promise for increasing ferroelectric polarization. These dipoles are thought to enhance nucleation and growth of the ferroelectric domains[34]. Further experimental characterization of thin films combined with theoretical understanding is needed to explain these phenomena for low dopant concentrations in a perovskite host as well as evaluation of the reliability of such perovskite solid solutions.

New ferroelectric materials are needed for FeRAM which have polarization values on the order of PZT and higher that are easily processed for device considerations. In addition, these should be lead free due to environmental concerns for European regulations. Examples of lead free materials are shown in the literature[35-36].

2. Reliability of ferroelectric capacitors

2.1 PZT thin film capacitor reliability

In order to circumvent aging phenomena or change in the electrical characteristics versus time and degradation phenomena in electroceramic materials it is essential that degradation mechanisms be understood as well as effective counter measures employed to avoid

degradation. In the case of PZT capacitors the use of metal oxide electrodes has led to orders of magnitude improvement in the endurance or cycling capability[37]. Although the oxide electrodes do show improved properties, the reason why they improve the ferroelectric properties still remains unclear. According to first principle calculations Pt electrodes form a better interface with ferroelectric films but in actual capacitors, the reliability of capacitors is much higher with a metal oxide electrode. (A recent paper on this topic indicates that flexoelectric coupling, i.e. strain-gradients, must be considered when simulating the interface between the dielectric and electrode layers by first principles as reported in, M. S. Majdoub, R. Maranganti, and P. Sharma, Phys. Rev. B 79, 115412-1-8 (2009)). Pt is a catalyst material and can reduce the near-by interface in low O_2 ambients which then would create a paraelectric layer at the electrode interface[38]. This type of paraelectric or dead-layer is one of the proposed reasons why ferroelectric capacitors degrade[12].

In the case, of piezoelectric devices improvement in the reliability of piezoelectric actuator was observed by application of potential to an oxide electrode in an actuator. And the authors demonstrated that classical polarization-loss phenomena could be nearly eliminated by this effective countermeasure[39]. These results indicate that issues such as hydrogen degradation phenomena in ferroelectric devices and long term reliability are inter-related[40-42]. It appears that some of the degradation phenomena in these types of devices is driven a electrochemical-physical phenomena especially when H_2O (vapor) or OH is present[43].

Recently, there have been fewer publications on reliability of PZT based ferroelectric capacitors for memory applications[44-51]. Since FeRAM has gone into large scale production reports on reliability from FeRAM from manufacturer is now limited compared with the 5-10 years ago. Therefore, industry's homepage is another source of information on this topic. Academic groups continue to work on endurance issues such as modeling fatigue[52]. In addition phase-field modeling of the capacitor shear stress when switching (111) oriented PZT film capacitors has explained switching irregularities[53] It has been proposed that the presence of a paraelectric layer at the interface is the reason for fatigue or loss of functionality in ferroelectric capacitors. Therefore decreasing this layer thickness is one way to improve reliability but again characterization of the interface is a challenge.

2.2 In-situ characterization of ferroelectric and piezoelectric properties

In-situ XRD which uses a focused synchrotron x-ray beam has shown promise in mapping micro-diffraction relationships of ferroelectric films in capacitors while applying nanosecond order electrical pulses which switch the domains[54-55]. This technique also lends itself to exploring degradation mechanism since the measurements can be done while switching in and changes in the lattice are measured in real-time. Piezoelectric force microscopy (PFM) has also been used for mapping the ferroelectric domain activity on micron-size capacitors[56]. Of the two techniques PFM has better small scale resolution but mapping or scanning the surface takes several minutes. The focused XRD beam requires a synchrotron and detailed knowledge of X-ray optics which is not ready available for the average researcher. The in-situ XRD probing has been limited to epitaxial films whereas with PFM polycrystalline films can also be characterized.

On key issue in ferroelectric memories has been trying to increase the memory density by creating a one transistor type memory. This type of memory appears very attractive but its non-volatile or charge retention characteristics has been a bottle neck. Research on developing a new materials with lower dielectric constants for using the Metal/Ferroelectric/Insulator/Semiconductor (MFIS) structure have so far been unable to obtain long term data storage. The problem with this of memory appears to be a combination of issues such as the quality of the interface between the ferroelectric and insulator and depolarization field[57-58].

2.3 Paraelectric thin films and their properties, crucial for the performance of decoupling capacitors and variable capacitance devices

From the general class of ferroelectric materials, the particular class of $(Ba_xSr_{1-x})TiO_3$ (BST) solid solutions, and more specifically the paraelectric BST thin films have been under development for nearly two decades.

Initially, they were used for the manufacturing of high density miniaturized or integrated thin film decoupling capacitors. During the last decade interest in BST film properties increased additionally because of their potential use in tunable microwave applications attested to the large variation of their dielectric constant with changes in DC bias fields, i.e., strong voltage tunability as well as the fact that the capacitance nonlinearly decreases with the increase of DC bias voltages. Much research has focused on strain effects and the influence of substrate on BST thin films properties, e.g.: how lattice structure distortions affect the direction and the magnitude of polarization formation and what is the response to an applied electric field.

Historically, the research activities in BST films deposition started in Japan more than two decades ago lead by the NEC[59]. BST thin films were directly deposited from a BST target by RF-sputtering and/or ion beam assisted deposition (IBAD) on r-cut sapphire substrates with Pt, Ru or RuO_2 electrodes, and the initially obtained dielectric constants were in the range of 820-880 for 475 nm thick $Ba_{0.5}Sr_{0.5}TiO_3$ film deposited at 600℃ with a sputtering pressure of 10 mTorr with O_2/Ar gas ratio of 1:10[59-60]. Many additional reports followed during the next decade when the metal organic decomposition (MOD), also called chemical solution deposition (CSD), became the most commonly used method for BST films fabrication. Few comprehensive reviews on CSD technique have been published, providing further details on the mechanism of film crystallization, and tailoring of microstructure through manipulation of deposition parameters[61-63]. In the present review the main focus will fall on the BST films obtained by RF-sputtering since very few review papers have systematically summarized the sputtered films properties data obtained in the last two decades[64-65], the only exception being the review on BST thin films for DRAM applications which to some extend covers the sputtered BST film performances, but the data included mentions limited papers published before the year 2000[66].

During the 90's very high deposition temperatures (e.g., 750-800℃) were required to achieve RF sputtered BST films with high dielectric constant BST, followed by additional post-deposition anneals also at high temperatures (750-900℃) in order to maintain low leakage currents[67-69]. An exception is the report of $Ba_{0.5}Sr_{0.5}TiO_3$ films deposited at 600℃ on Pt/TiO_2/SiO_2/Si substrates, claiming that a dielectric constant as high as 638 was obtained from 96-120 nm thick BST films[70-71]. Conditions for sputter deposition included O_2/Ar ratio gas flow ratio of 1:3, a power ratio of rf/pulse dc of 800 W/200 W, and a deposition rate of 55 Å/min. In a different report several years later, a similar set-up was used but with different deposition conditions, concluding that the BST films needed to be deposited at 800℃ on the same type of substrates in order to get dielectric constant close to 521-555, regardless of the (Ba+Sr)/Ba ratio used[72]. It was also reported that a dielectric constant of 600, obtained from BST films grown by RF sputtering at 650℃ with 200 nm thickness and such BST films had (111) oriented large grains (average grain size of 300nm) with (200/100) reflections also present[73-74].

During the last decade, additional research on sputtered BST films was conducted by Argonne National Laboratory (ANL)[75-76], which utilized a very different approach for the RF sputtering deposition of BST films. It consisted of three stages. First, a thin BST layer (~5nm) with a (Ba+Sr)/Ti ratio of 0.73 was deposited at room temperature on top of the Pt bottom electrode (Pt/TiO_2/SiO_2/Si) to prevent the appearance of surface roughening and/or hillocking effects associated with the limited stability of the Pt bottom electrodes at high temperatures and/or under high oxygen partial pressures.[77-78] Second, a 60nm main BST layer with a (Ba+Sr)/Ti ratio of 0.9 was deposited at 650℃ onto the initial layer. Finally, another Ti-rich BST, (Ba+Sr)/Ti = 0.73, top interfacial layer was deposited onto the multilayered BST at 650℃. All three BST layers were deposited in the same vacuum chamber, using a single stoichiometric $Ba_{0.5}Sr_{0.5}TiO_3$ ceramic target.[75] Single layer sputtered BST film with the thickness of 70 nm had dielectric constant of 520 and tunability close to 3:1 under 1MV/cm electric field[75], however, the heterostructured BST films exhibited relatively low dielectric constant (~170), but did show significant improvement of the dielectric breakdown field[76]. The main limitation of the ANL deposition process is the relatively high sputtering pressure of 55 mTorr, which results in a reduction of the deposition rate to 5Å/min with O_2/Ar gas ratio in the 1:1-1:5 range[75-76]. Other

studies determined that the off-axis sputtered BST films do have lower dielectric constants than the on-axis sputtered ones[79] due to the higher in-plane compressive stress. On-axis sputtered $Ba_{0.44}Sr_{0.56}TiO_3$ film with 138 nm thickness grown at 410℃ had dielectric constant close to 400 under 50mTorr sputtering pressure and O_2/Ar gas ratio 1:4 on Pt/SiO_2/Si substrate. The same study also concluded that off-axis sputtered BST films possess larger leakage current density due to the severe ion bombardment during the film growth, which potentially causes a higher concentration of charged defects, such as oxygen vacancies.[79]

So far it is commonly accepted that there are several main factors controlling the tunability of polycrystalline BST thin films. Firstly, the in-plane strain of the BST films caused by the mismatch of thermal expansion coefficients between the BST films ($\approx 10\times 10^{-6}$/℃) and the thermal expansion coefficients of the substrates upon which they have been deposited. Secondly, the impact of the BST film preferential crystal orientation, e.g., BST films with one-axis (110), (100) or (111) predominant orientations on film dielectric properties. This second factor has not been fully clarified so far unlike the other commonly studied ferroelectric thin films (e.g., PZT, SBT, etc.), because of the variety of seed layers and/or substrates typically applied to achieve the required preferential orientation, not underestimating the influence coming from the bottom electrode and/or seed layer, i.e.: the difference in the interfacial structure and the barrier height of seed/buffer layers, the interdiffusion to the BST dielectric properties, all of which is not separable from the contribution of the BST film preferential crystal orientation on the polarizability[80]. Few recent attempts to clarify the above interactions are reported in studies concerning the effect of purely (111) and (100)-oriented BST films on the voltage tunability for BST films grown on substrates with different bottom electrode layers stacks, e.g., $LaNiO_3$, $SrRuO_3$, $LaSrCoO_3$, IrO_2, Pt, etc. and their combinations[80]. These electrically conductive oxide electrode layers can lower the required crystallization temperature during the BST films growth, but they may contribute to additional modification of the interfacial dielectric properties of the BST films near the electrodes. This latter factor is most commonly used to control the voltage tunability in BST films through the crystal habit and grain size, the Ba/(Ba+Sr) ratio, typically from 0.25 to 0.70, and the film growth temperature and/or post-annealing temperature, typically from 600℃ to 900℃. An additional key factor for both RF-sputtering and pulse laser deposition (PLD) is the oxygen partial pressure and total deposition pressure. RF-sputtering studies are usually conducted at higher oxygen partial pressures (10−50% of O_2 in Ar), which requires higher sputtering pressures (>50mTorr) to ensure close to stoichiometric (Ba+Sr)/Ti ratio of the films during the high temperatures (600− 800℃) deposition. BST films sputtered with higher $O_2/(O_2+Ar)$ ratios tend to have higher dielectric constant and lower leakages currents, but still lack sufficiently high tunability, even when the BST layers were grown on $LaNiO_3$/Pt bottom electrodes. Systematic investigation of the process deposition parameters window covering wide ranges of deposition pressures and oxygen partial pressures, both exercising a strong influence on the dielectric properties of the BST films grown by PLD on MgO substrates, were recently conducted by J. Hiltunen *at al.*[81]. An equivalent report for RF-sputtered BST films is not yet available, but will hopefully appear in the near future. Without such a systematic study at hand, few investigations conclude that it is not by RF-sputtering[82] but by PLD that higher than 1000 dielectric constants of the BST films grown on MgO substrates can be achieved. It is not easy to judge if such observation derives from the fundamental differences during the film growth using two processes or if it originates from the narrow process windows used for the RF sputter deposition for those BST films in particular.

Presently, many attempts have been made to utilize the proper combination of the most favorable trade-offs between all of the above key factors and interactions for polycrystalline BST films deposited by any method with thicknesses from 100 nm to 300 nm. Unfortunately, tunability ratios of higher than 3:1 for C(0V)/C(40 V/μm) and higher than 5:1 for C(0V)/C(150 V/μm), were never simultaneously obtained, thus failing the requirements of low dielectric loss, <1% or preferably less than 0.5% at 1KHz (or alternatively Q>100 at 1GHz), and of low leakage current densities under such high electric fields. In addition, for practical applications, the capacitance tunability should be between 4.5:1 to 6.5:

1 or better, which is achievable within DC tuning voltages from 2V to 12V (for the BST case, it could be from 0.5V to less than 10V to have the same ΔV=10V) in order to be able to compete with modern GaAs varactors[83-84]. Table 2 provides a detailed summary of the reported polycrystalline BST films with highest tunabilities and their measured or estimated FOM and CQF for 0.5-1.0 GHz frequency range. The BST film properties summarized in Table 2 are selected from reports in which the deposition substrates can be made available in large sizes and can be used for commercial applications, such as Si and Al_2O_3[85-92]. Apparently, there is no reported data for FOM higher than 75, with a single exception of FOM estimated at 116, and the CQF always being lower than 40,000. As it can been seen from Table 2, very few BST films can get close enough to the requirements in order to posses actual performance advantages compared to the GaAs varactors. The case of 100 nm sputtered BST films with Ba/(Ba+Sr) = 0.7 on Al_2O_3 substrates, with dielectric constant close to 800, tunability of 4.5 : 1 from 0V to 7V (70V/μm) and 6 : 1 from 0V to 10V (100V/μm), with tan δ of 2% at 1KHz or at 0.5GHz, with figure of merit (FOM) and commutation quality factor (CQF) of 42 and 27192 respectively[90] is such an example, as well as the case of 800nm sputtered BST films with Ba/(Ba+Sr)=0.6 on Ni foils, post-annealed at 900℃, with dielectric constant of 1800, tunability of 10 : 1 from 0V to 35V (44V/μm), with tan δ of 1.2% at 10KHz and highest possible FOM of 75[92]. The tunability of $Ba_{0.6}Sr_{0.4}TiO_3$ film (~300nm) deposited on Pt/Ti/SiO_2/Si(100) substrate with a $La_{0.7}Sr_{0.3}CoO_3$ buffer by pulse laser deposition (PLD) at 800℃ is 4.0 : 1 from 0V to 7.5V (25V/μm)[91] (see Fig. 3).

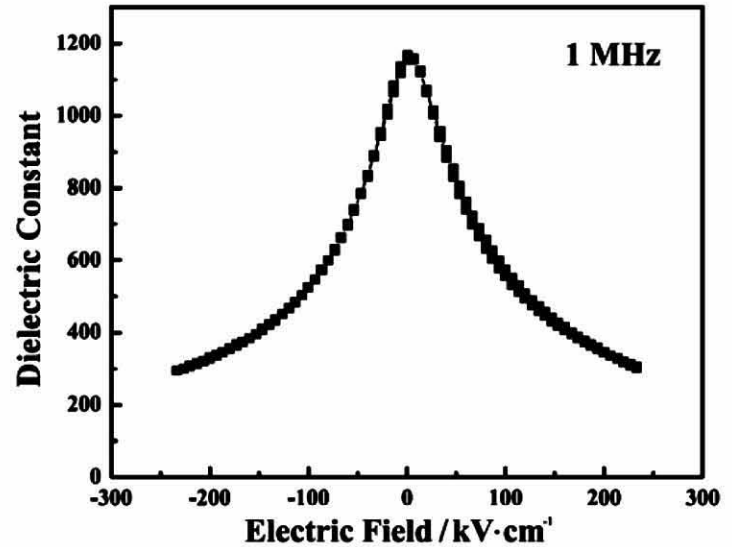

Fig. 3 Dielectric constant of $Ba_{0.6}Sr_{0.4}TiO_3$ film (~300nm) deposited on $La_{0.7}Sr_{0.3}CoO_3$/Pt/Ti/SiO_2/Si (100) substrate as a function of the applied dc bias field measured at room temperature [91] (see also Table 2). (© 2009 American Institute of Physics)

2.4 Reliability related to (Ba,Sr)TiO_3 parallel-plate (Pt/BST/Pt (MIM)) thin film capacitors

In respect to the reliability of BST capacitors, it is important to conduct lifetime measurements after the completion of all processing steps for the fabrication of the decoupling or tunable metal-insulator-metal (MIM) capacitors. In addition, there are other quantitative methods of reliability assessment, such as resistance degradation, time dependent dielectric breakdown (TDDB) and electrical Stress-Induced Leakage Current

Table 2 Selected examples of dielectric properties reported for BST films at frequency of 1-100KHz and/or 0.5-1GHz and their estimated or figures of merit, commutation quality factors and voltage tunabilities

Dielectric, Electrode and Substrate Materials	Deposition method	BST Thickness nm	Capacitance Density @ 0V fF/μm²	Dielectric constant @ 0V	Electric Field V/μm	DC Bias V	Tunability C(0V)/C(V)	tan(δ) @ 0V KHz or GHz	tan(δ) @ V KHz or GHz	FOM max	CQF max	Reference
BST90/10:BST75/25:BST60/40 /Pt/Si	MOD/CSD	225	14.2	360	44	10	3.0	0.013	0.008	53	14222	[85]
$Ba_{0.5}Sr_{0.5}TiO_3$/$SrRuO_3$/Pt/Al_2O_3	RF sputter	210	27.4	650	30	6.3	2.9	0.015	0.025	44	3293	[86]
$Ba_{0.6}Sr_{0.4}TiO_3$/Pt/Au/Si	PLD	250	26.6	750	32	8	3.8	0.025	0.024	29	3433	[87]
$Ba_{0.65}Sr_{0.35}TiO_3$/$LaNiO_3$/Pt/Si	MOD/CSD	352	44.0	2000	23	8	2.7	0.035	0.012	18	2480	[88]
BST/Pt/ST/LSCO/CeO2/YSZ/Si	PLD	200	55.3	1250	25	5	2.3	0.025	0.013	22	2281	[89]
$Ba_{0.5}Sr_{0.5}TiO_3$/Pt/TiO_x/SiO_2/Al_2O_3	MOD/CSD	100	26.3	297	100	10	3.7	0.006	0.008	116	39461	[90]
$Ba_{0.7}Sr_{0.3}TiO_3$/Pt/TiO_x/SiO_2/Al_2O_3	MOD/CSD	100	41.1	464	100	10	5.3	0.016	0.009	52	23314	[90]
$Ba_{0.7}Sr_{0.3}TiO_3$/Pt/TiO_x/SiO_2/Al_2O_3	RF sputter	100	70.0	791	100	10	6.3	0.020	0.008	42	27192	[90]
$Ba_{0.6}Sr_{0.4}TiO_3$/$La_{0.7}Sr_{0.3}CoO_3$/Pt/Si	PLD	300	35.4	1200	25	7.5	4	0.010	-	75	-	[91]
$Ba_{0.6}Sr_{0.4}TiO_3$/Ni foil	RF sputter	800	19.9	1800	44	35	10	0.0120	-	75	-	[92]

(SILC). It is important to measure the breakdown time as a function of the applied voltage and to predict by extrapolation the lifetime of MIM capacitor structures under typical operation voltages, e.g., 2−4 Volts. Such lifetime measurements are commonly conducted under voltages not higher than 1/2 of the typical breakdown voltage, i.e., for 100-150 nm thick nm BST, typical breakdown voltages are in the 25-32 Volts[93] range, assessed under high temperature bias stress from 85℃ to 175℃.

Some preliminary studies on voltage tunable interdigitated electrode (IDE) type planar BST structures were conducted under 300×106 of switching cycles with an amplitude of 150V, frequency of 1kHz, and under constant high DC bias condition, have shown some reduction of the voltage tunability, but the obtained results have not been compared with Pt/BST/Pt (MIM) structures[94]. The MIM tunable capacitor structures are complex to assess because they require multiple fabrication steps to complete, such as patterning and ion-milling, application of interlayer dielectric (ILD) single stack or multiple stacks, passivation hermetically sealing layer, e.g. SiN_x, etc., and single or double metal interconnects, before elevated temperature or humidity bias conditions can be applied to them. The reliability of the parallel-plate BST capacitors tested with high electric fields for the required capacitance tunabilities is yet to be evaluated. Reliability studies of 150nm BST deposited by RF sputtering at very low temperatures on polyimide resin coated Si wafers and of Pt/BST/Pt integrated capacitors with Al_2O_3 barrier layers were conducted by using both a pressure cooker test (PCT) under 121℃, 85%RH for 336 hours and a thermal cycling test (TCT) varying the temperatures from −65℃ to 125℃ for 500 cycles.[95] Due to the very low dielectric constant and the amorphous nature of the BST films they did not exhibit dielectric breakdown and resistance degradation at room temperature for applied voltages from −50 to 50V with leakage current density as low as 10^{-9}A/cm^2 at 10V.[95]

Recent reliability studies of Pt/BST/Pt MIM (Ba/(Ba+Sr)=0.6) tunable capacitors deposited by combination of MOD/CSD and RF sputtering methods on Al_2O_3 substrates, have shown reduction of the voltage tunability by approximately 2−3% from the original 3.4:1 value under constant voltage stress of 10V after 100 hours of TDDB test at 125℃.[96] A similar trend is also observed for the capacitance value at zero DC bias for BST capacitors under constant voltage stress after the first 100 hours, but without further degradation afterwards up to 1000 hours of the TDDB testing. Some space charge phenomena at the electrode interfaces were assigned as a controlling mechanism of the DC bias tuning changes of the BST capacitors under constant voltage stress.[96] The voltage tunability changes, on the other hand, could be related to the reported positive voltage shift in the C-V curves of Pt/BST/Pt MIM capacitors after stress biasing which is associated with the accumulation of positively charged ionic defects at the bottom BST/Pt (cathode) electrode interface of the capacitors.[97-99] Further key insights on the effects of post-annealing atmosphere on the BST film dielectric constant and the C-V curves can be found in the work of F. M. Pontes *et al.*[100] Another recent comprehensive review covering both microwave BST tunable devices and high density thin film decoupling capacitors, their design, properties and reliability was completed by a research group at Chalmers University of Technology in Sweden.[101] The review documents the performance challenges including non-recovery to zero bias capacitance after application of the large DC biases and slow relaxation time at the interfaces of Pt/BST/Pt MIM capacitors.[101]

Further studies are necessary to determine the optimal conditions for obtaining polycrystalline BST film with superior properties using different deposition techniques on the same substrates, with the same electrode stack/seed layers, under the same temperatures, and the same compositions and thicknesses, thus establishing with a reasonable level of certainty the true limit of their dielectric and microwave properties as well as their reliability.

As noted above materials-device analysis is a complicated topic. In Japan, reliability engineering is not routinely taught at universities since it is more associated with manufacturing and product testing. We believe that educating engineering students at Universities in Japan need to impart to them a greater understanding of materials engineering reliability, design and data analysis of complex material-device systems in order for them to make greater contributions to this field[102-104].

3. Conclusions

In this review, a bird's eye view of the ferroelectrics film based devices was presented and challenges they face were reported. In particular, PZT based capacitors for ferroelectric memory applications as well as BST characteristics vs. processing conditions was examined for use in charge storage devices. Further investigation on topics such as the interface, scaling, reliability, and new materials are needed to advance the field. Finally, accurate measurements of ferroelectric based capacitors electrical properties is not a trivial matter as noted in the literature[9].

In general, we believe a more holistic approach is needed when evaluating thin film materials in a numerical or quantifiable manner in order to allow greater comparisons within the literature and solving fundamental problems which have plagued ferroelectric based devices for decades.

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